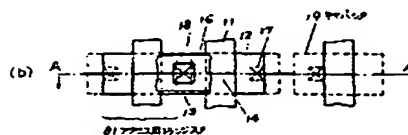
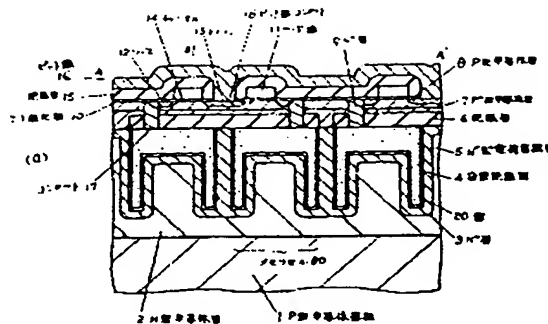


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APPLICANT : MATSUSHITA ELECTRIC IND CO LTD;  
INVENTOR : YASUI TAKATOSHI;  
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TITLE : SEMICONDUCTOR MEMORY DEVICE  
AND MANUFACTURE THEREOF



ABSTRACT : PURPOSE: To provide an excellent memory cell having minimum deterioration in dielectric strength and high long-term reliability by providing a semiconductor layer of a second conductivity type in a region of a semiconductor substrate of a first conductivity type where a memory cell is to be formed, forming grooves in the semiconductor layer, forming a capacity insulating film on the surface of the grooves and providing a charge storing layer of the second conductivity type having high dopant concentration within the grooves for defining a capacitor.

CONSTITUTION: An N-type semiconductor layer 3 is formed in a region of a P-type semiconductor substrate 1 where a memory cell 80 is to be formed. The N-type semiconductor layer 2 is provided with grooves such that a part of the N-type semiconductor layer 2 is left between the grooves like an island. An N<sup>+</sup> type layer 3 is formed on the surface of the grooves 20 by ion implantation or diffusion. A capacity insulating film 4 is formed on the surface of the grooves 20 and an N<sup>+</sup> type charge storing layer 5 is formed within the grooves 20 having the capacity insulating film 4. A capacitor 19 is defined by these components and an accessing transistor 81 is formed over the capacitor 19. The accessing transistor 81 includes a P<sup>+</sup> type semiconductor layer 7, a P-type semiconductor layer 8, a gate oxide film 10 and word lines 11 all of which are formed over an insulating layer 6 and the transistor 81 further includes N<sup>+</sup> type source and drain 12, 13 formed in the P-type semiconductor layer 8.

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